Techniques to Reduce Solder Voiding Under BTC Components

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Abstract

Reducing solder voiding under BTC components is a large problem facing industry especially with the increase in the number of components being designed that require greater thermal requirements. Various techniques can be used to reduce voiding which include the design of the PCBA, the type of attachment materials used and the assembly equipment. This poster will show how the use of vias and a soldermask grid on the land pad can reduce the overall size of the voids and total voiding in solder attachment. Testing was performed using a FR4 substrate shown in Figure 1 incorporating SOT89, 3x6DFN, 4x4QFN and 5x5QFN packages. Results shown in Figures 2 and 3 show how adding the vias and the soldermask grid can influence the amount of voiding and potentially reduce the amount of voiding to less than 20%. Additional results will be provided on the use of meshed preforms to attach BTC components such as the attachment of a ceramic package directly to a heatsink and the effects of the overall stack-up on the solder attach results. The use of the meshed preforms to control the volume of solder while selecting the proper flux coating reduced the overall voiding to less than 10%. Future work on the effects of advanced heatsinking in substrate fabrication for higher power packages will be outlined. Some of the various assembly equipment advances to help reduce solder voiding will be mentioned. Also how IPC has a document, IPC-7093 for the Design and Assembly Process Implementation for Bottom Termination SMT Components.

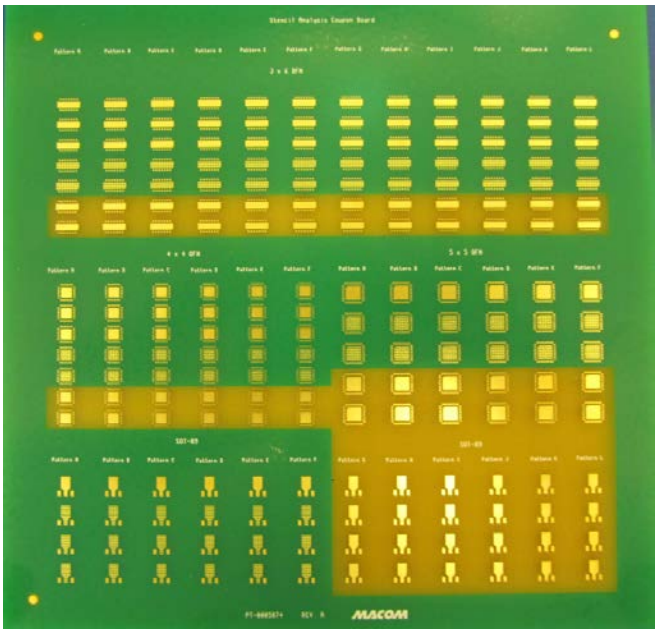

Fig: 1 FR4 Test Vehicle

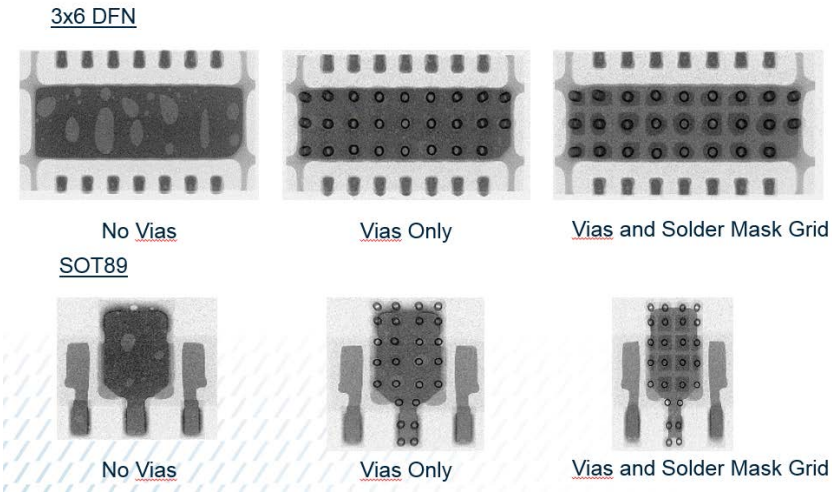

Fig 2: 3x6DFN and SOT89 X-ray Results

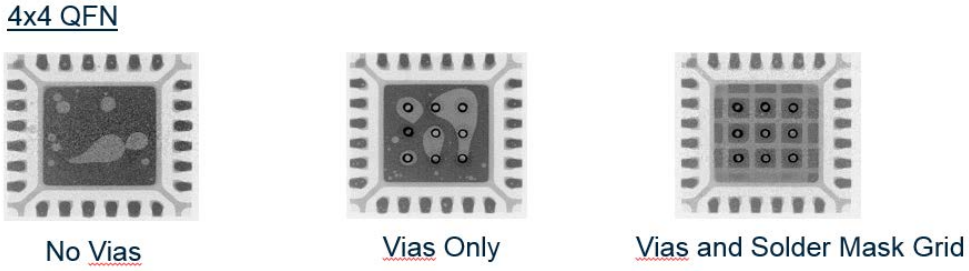

Fig 3: 4x4 QFN X-ray Results